WHAT IS CLAIMED IS:

1. A single chip set-top box integrated circuit, comprising:

a digital BTSC encoder that is operable to encode first and second digital audio signals into a BTSC encoded signal, said first and second digital audio signals having a bandwidth defined by the frequency content of said signals; and

a digital output modulator for receiving the BTSC encoded signal and generating a modulated output signal that is provided off chip;

wherein the digital BTSC encoder and digital output modulator are formed together on a common substrate.

2. The single chip set-top box integrated circuit of claim 1, wherein:

the digital BTSC encoder comprises (a) a sum channel processor comprising a first digital filter for digitally processing a digital sum signal and (b) a difference channel processor comprising a second digital filter for digitally processing a digital difference signal, wherein the digital BTSC encoder operates at a sample rate that is at least substantially ten times the bandwidth of the first and second digital audio signals so that said digital filters in the sum channel processor and the difference channel processor substantially match BTSC analog filter transform functions in both magnitude and phase; and

the digital output modulator comprises an audio/video processor that is operable to encode an audio/video signal thereby generating a Radio Frequency (RF) modulated audio/video signal as the modulated output signal.

3. The single chip set-top box integrated circuit of claim 2, wherein the RF modulated audio/video signal is a channel 3/4 RF modulated audio/video signal that is provided off chip to at least one audio/visual playback device.

4. The single chip set-top box integrated circuit of claim 2, further comprising:

a rate converter and FM modulator, communicatively coupled to the audio/video processor, that modulates the BTSC encoded signal, thereby generating a processed audio signal; and

a video processor, communicatively coupled to the audio/video processor, that performs video processing of a composite video signal thereby generating a processed video signal;

wherein the audio/video processor combines the processed audio signal and the processed video signal into the audio/video signal.

5. The single chip set-top box integrated circuit of claim 1, wherein the first and second digital audio signals are Pulse Code Modulation (PCM) baseband audio source signals.

6. The single chip set-top box integrated circuit of claim 2, wherein the digital output modulator comprises a Digital to Analog Converter (DAC) that is operable to transform a digital signal into an analog signal.

7. The single chip set-top box integrated circuit of claim 6, comprising a high speed clock generator for generating a first clock signal for clocking the DAC and for generating a second clock signal for clocking high speed digital logic that transfers data to the DAC.

8. The single chip set-top box integrated circuit of claim 7, wherein the first and second clock signals have a phase relationship that is controlled by a phase control signal.

9. The single chip set-top box integrated circuit of claim 1, wherein the digital BTSC encoder and a digital output modulator are formed together on a common silicon substrate using CMOS processing.

10. The single chip set-top box integrated circuit of claim 1, comprising an output for providing the modulated output signal off chip to at least one audio/visual playback device.

11. An integrated circuit that includes a digital audio/video system, the integrated circuit comprising:

(A) a digital audio processor for BTSC encoding first and second digital audio signals into an encoded audio signal, comprising sum channel processing means and difference channel processing means;

(B) a digital video processor that processes a composite video signal, thereby generating a digital video signal; and

(C) an audio/video processor that is operable to modulate the encoded audio signal and digital video signal to generate a Radio Frequency (RF) modulated audio/video signal that is provided off chip,

wherein the digital audio processor, digital video processor and audio/video processor are formed together on a common substrate.

12. The integrated circuit of claim 11, wherein the digital audio processor operates at a sample rate so that said sum channel processing means and the difference channel processing means substantially match BTSC analog filter transform functions in both amplitude and phase whereby substantially no phase compensation is required.

13. The integrated circuit of claim 11, wherein:

the digital audio processor is communicatively coupled to the audio/video processor and performs audio processing on a Pulse Code Modulation (PCM) baseband audio source signal to generate the encoded audio signal;

the digital video processor is communicatively communicatively coupled to the audio/video processor to generate the digital video signal; and

the audio/video processor combines the encoded audio signal and the digital video signal into the audio/video signal.

14. The integrated circuit of claim 11, wherein the audio/video processor comprises a DAC that is clocked with a very high speed clock signal.

15. The integrated circuit of claim 14, comprising a clock generator for generating the very high speed clock signal and for providing a second clock signal to

digital logic circuitry that transfers data to the DAC, wherein a timing relationship between the very high speed clock signal and the second clock signal is programmably controlled.

16. The integrated circuit of claim 11 integrated as part of a single chip set-top box comprising an IF demodulator, a video decoder, a transport processor, a digital audio processor, a high-definition MPEG video decoder, a BTSC decoder and an audio DAC.

17. The integrated circuit of claim 11, wherein the digital audio processor is communicatively coupled to a BTSC decoder that operates cooperatively with the integrated circuit to support BTSC decoding, whereby data can be exchanged between the digital audio processor and the BTSC decoder to co-verify said data using an all digital loopback mode.

18. The integrated circuit of claim 11, wherein the digital audio processor operates at a sample rate that is at least approximately ten times the bandwidth of the first and second digital audio signals so that no phase compensation is required in the sum channel processing means or difference channel processing means to substantially match BTSC analog filter transform functions in both magnitude and phase.

19. A method for modulating an audio/visual signal on a single integrated circuit chip, comprising:

receiving audio data and video data on the chip;

digitally processing the video data on the chip to generate a composite video signal;

digitally encoding the audio data on the chip in accordance with an audio encoding standard;

converting the baseband encoded composite signal from a first sampling rate to a second sampling rate on the chip;

frequency modulating an aural carrier using the converted baseband encoded composite signal on the chip, thereby generating an FM modulated audio signal;

mixing the composite video signal and FM modulated audio signal to a programmable carrier frequency on the chip, thereby generating an RF modulated audio/visual signal; and

outputting the RF modulated audio/visual signal off chip.

20. The method of claim 19, wherein the RF modulated visual signal is a channel 3/4 RF modulated audio/video signal.

21. The method of claim 19, wherein the step of digitally encoding the audio data comprises using a sampling rate of at least approximately 150-200 kHz to generate a baseband encoded composite signal.